REMARKS

Claims 1-14 are pending in the present application.

I. Rejection under 35 U.S.C. §102(b)

Claims 1-14 have been rejected under 35 U.S.C. §102(b) as being anticipated by Morley (US-A-4,276,594). This rejection under 35 U.S.C. §102(b) is respectfully traversed.

A. Independent Claim 1

With respect to independent claim 1, the Examiner alleges that Morley discloses fetching a program instruction from the unified memory; determining if the fetched program instruction would require three unified memory accesses during a single instruction cycle; accessing the unified memory a first time, during the instruction cycle associated with the fetched program instruction, with a dummy access; fetching a next program instruction from an instruction register, during the instruction cycle associated with the fetched program instruction; and accessing the unified memory a second time, during the instruction cycle associated with the fetched program instruction, with a data access. From the allegations, the Examiner concludes that the presently claimed invention of independent claim 1 is anticipated by the teachings of Morley.

As noted above, the Examiner alleges that Morley discloses determining if the fetched program instruction would require three unified memory accesses during a single instruction cycle and points to column 58, lines 17-20, of Morley to support the allegation. Column 58, lines 17-20, states:

> The 6800 accesses this RAM during the PHΦ of the MIO cycle. During serial I/O, this time is used to fetch/store characters and update pointers. For parallel I/O, this is used to fetch parameters for the PIA.

Contrary to the Examiner' position, this passage of Morley fails to discuss or disclose any determination with respect to the number of unified memory accesses that would be required during a single instruction cycle. Thus, this passage of Morley cannot provide any basis for a finding of anticipation to the limitation corresponding to determining if the fetched program instruction would require three unified memory accesses during a single instruction cycle for proper execution of the fetched program instruction, proper execution of the fetched program instruction being the microprocessor performing operations requested by the fetched program instruction in a single instruction cycle of independent claim 1.

Column 58, lines 17-20, of Morley merely teaches that the RAM may include a parallel I/O port. Column 58, lines 17-20, of Morley is void of any teachings directed to determining if the fetched program instruction would require three unified memory accesses during a single instruction cycle for proper execution of the fetched program instruction, proper execution of the fetched program instruction being the microprocessor performing operations requested by the fetched program instruction in a single instruction cycle, as set forth by independent claim 1.

Moreover, as noted above, the Examiner alleges that Morley discloses accessing the unified memory a first time, during the instruction cycle associated with the fetched program instruction, with a dummy access and points to column 58, lines 17-20, of Morley to support the allegation.

Contrary to the Examiner' position, this passage of Morley fails to discuss or disclose any type of dummy access of the unified memory. Thus, this passage of Morley cannot provide any basis for a finding of anticipation to the limitation corresponding to accessing the unified memory a first time, during the instruction cycle associated with the fetched program instruction, with a dummy access of independent claim 1.

As noted above, column 58, lines 17-20, of Morley merely teaches that the RAM may include a parallel I/O port. Column 58, lines 17-20, of Morley is void of any teachings directed to accessing the unified memory a first time, during the instruction cycle associated with the fetched program instruction, with a dummy access, as set forth by independent claim 1.

Lastly, as noted above, the Examiner alleges that Morley discloses accessing the unified memory a second time, during the instruction cycle associated with the fetched program instruction, with a data access and points to Figure 28 to support the allegation.

With respect to Figure 28, the read operation illustrates that during the PHΦ of the MIO cycle, the data from the memory is accessed and place on the bus; during the PH1 of the MIO cycle, the data sits on the bus; and during the PH2 of the MIO cycle, the data on the bus is uploaded or read. Thus, the memory is only access once per MIO cycle and fails to anticipate accessing the unified memory a second time, during the instruction cycle associated with the fetched program instruction, with a data access, as set forth by independent claim 1.

B. Independent Claim 6

With respect to independent claim 6, the Examiner alleges that Morley discloses fetching a program instruction from the unified memory during a first instruction cycle; determining if the fetched program instruction for a second instruction cycle is a conditional program code discontinuity; accessing the unified memory a first time during the second instruction cycle with a dummy access when it is determined that the program instruction accessed for a second instruction cycle is a conditional program code discontinuity; and accessing the unified memory a second time during the second instruction cycle to read a new instruction when it is determined the program instruction accessed for a second instruction cycle is a conditional program code discontinuity, thereby delaying the instruction access from the unified memory for the second instruction cycle by a half cycle. From the allegations, the Examiner concludes that the presently claimed invention of independent claim 6 is anticipated by the teachings of Morley.

As noted above, the Examiner alleges that Morley discloses determining if the fetched program instruction for a second instruction cycle is a conditional program code discontinuity and points to column 58, lines 17-20, of Morley to support the allegation. Column 58, lines 17-20, states:

> The 6800 accesses this RAM during the PHΦ of the MIO cycle. During serial I/O, this time is used to fetch/store characters and update pointers. For parallel I/O, this is used to fetch parameters for the PIA.

Contrary to the Examiner' position, this passage of Morley fails to discuss or disclose any determination with respect to the fetched program instruction for a second instruction cycle being a conditional program code discontinuity. Thus, this passage of Morley cannot provide any basis for a finding of anticipation to the limitation corresponding to determining if the fetched program instruction for a second instruction cycle is a conditional program code discontinuity of independent claim 6.

Column 58, lines 17-20, of Morley merely teaches that the RAM may include a parallel I/O port. Column 58, lines 17-20, of Morley is void of any teachings directed to determining if the fetched program instruction would be a conditional program code discontinuity, as set forth by independent claim 6.

Moreover, as noted above, the Examiner alleges that Morley discloses accessing the unified memory a first time during the second instruction cycle with a dummy access and points to column 58, lines 17-20, of Morley to support the allegation.

Contrary to the Examiner' position, this passage of Morley fails to discuss or disclose any type of dummy access of the unified memory. Thus, this passage of Morley cannot provide any basis for a finding of anticipation to the limitation corresponding to accessing the unified memory a first time during the second instruction cycle with a dummy access of independent claim 6.

As noted above, column 58, lines 17-20, of Morley merely teaches that the RAM may include a parallel I/O port. Column 58, lines 17-20, of Morley is void of any teachings directed to accessing the unified memory a first time during the second instruction cycle with a dummy access, as set forth by independent claim 6.

Lastly, as noted above, the Examiner alleges that Morley discloses accessing the unified memory a second time during the second instruction cycle to read a new instruction when it is determined the program instruction accessed for a second instruction cycle is a conditional program code discontinuity, thereby delaying the instruction access from the unified memory for the second instruction cycle by a half cycle and points to Figure 28 to support the allegation.

With respect to Figure 28, the read operation illustrates that during the PHΦ of the MIO cycle, the data from the memory is accessed and place on the bus; during the PH1 of the MIO cycle, the data sits on the bus; and during the PH2 of the MIO cycle, the data on the bus is

uploaded or read. Thus, the memory is only access once per MIO cycle and fails to anticipate accessing the unified memory a second time, during the instruction cycle associated with the fetched program instruction, with a data access, as set forth by independent claim 6.

C. Independent Claim 9

With respect to independent claim 9, the Examiner alleges that Morley discloses fetching a program instruction from the unified memory; determining if the fetched program instruction is a loop initiation instruction; storing a first instruction of the loop in an instruction register when the fetched program instruction is a loop initiation instruction; executing the loop; determining if a fetched instruction during the execution of the loop is a last instruction of the loop; accessing the unified memory a first time, during the instruction cycle associated with the fetched last instruction of loop, with a dummy access; fetching the first instruction of the loop from the instruction register, during the instruction cycle associated with the fetched last instruction of loop; and accessing the unified memory a second time, during the instruction cycle associated with the fetched last instruction of loop, with a data access. From the allegations, the Examiner concludes that the presently claimed invention of independent claim 9 is anticipated by the teachings of Morley.

As noted above, the Examiner alleges that Morley discloses accessing the unified memory a first time, during the instruction cycle associated with the fetched last instruction of loop, with a dummy access and points to column 58, lines 17-20, of Morley to support the allegation. Column 58, lines 17-20, states:

> The 6800 accesses this RAM during the PHΦ of the MIO cycle. During serial I/O, this time is used to fetch/store characters and update pointers. For parallel I/O, this is used to fetch parameters for the PIA.

Contrary to the Examiner' position, this passage of Morley fails to discuss or disclose any accessing the unified memory a first time, during the instruction cycle associated with the fetched last instruction of loop, with a dummy access. Thus, this passage of Morley cannot provide any basis for a finding of anticipation to the limitation corresponding to accessing the

unified memory a first time, during the instruction cycle associated with the fetched last instruction of loop, with a dummy access of independent claim 9.

Column 58, lines 17-20, of Morley merely teaches that the RAM may include a parallel I/O port. Column 58, lines 17-20, of Morley is void of any teachings directed to accessing the unified memory a first time, during the instruction cycle associated with the fetched last instruction of loop, with a dummy access, as set forth by independent claim 9.

Moreover, as noted above, the Examiner alleges that Morley discloses accessing the unified memory a second time, during the instruction cycle associated with the fetched last instruction of loop, with a data access and points to Figure 28 to support the allegation.

With respect to Figure 28, the read operation illustrates that during the PHΦ of the MIO cycle, the data from the memory is accessed and place on the bus; during the PH1 of the MIO cycle, the data sits on the bus; and during the PH2 of the MIO cycle, the data on the bus is uploaded or read. Thus, the memory is only access once per MIO cycle and fails to anticipate accessing the unified memory a second time, during the instruction cycle associated with the fetched program instruction, with a data access, as set forth by independent claim 9.

D. Independent Claim 13

With respect to independent claim 13, the Examiner alleges that Morley discloses accessing a program instruction from the unified memory during a first instruction cycle; determining a type of program instruction; pre-fetching a next instruction from the unified memory; saving the pre-fetched instruction in a register when it is determined that the type of program instruction is a first instruction of a loop; fetching a next instruction from the register when it is determined that the type of program instruction is a last instruction of a loop; accessing the unified memory with a dummy access during execution of the last instruction of the loop; and accessing the unified memory, a second time, with a data access during execution of the last instruction of the loop. From the allegations, the Examiner concludes that the presently claimed invention of independent claim 13 is anticipated by the teachings of Morley.

As noted above, the Examiner alleges that Morley discloses accessing the unified memory with a dummy access during execution of the last instruction of the loop and points to column 58, lines 17-20, of Morley to support the allegation. Column 58, lines 17-20, states:

> The 6800 accesses this RAM during the PHΦ of the MIO cycle. During serial I/O, this time is used to fetch/store characters and update pointers. For parallel I/O, this is used to fetch parameters for the PIA.

Contrary to the Examiner' position, this passage of Morley fails to discuss or disclose any accessing the unified memory with a dummy access during execution of the last instruction of the loop. Thus, this passage of Morley cannot provide any basis for a finding of anticipation to the limitation corresponding to accessing the unified memory with a dummy access during execution of the last instruction of the loop of independent claim 13.

Column 58, lines 17-20, of Morley merely teaches that the RAM may include a parallel I/O port. Column 58, lines 17-20, of Morley is void of any teachings directed to accessing the unified memory with a dummy access during execution of the last instruction of the loop, as set forth by independent claim 13.

Moreover, as noted above, the Examiner alleges that Morley discloses accessing the unified memory, a second time, with a data access during execution of the last instruction of the loop and points to Figure 28 to support the allegation.

With respect to Figure 28, the read operation illustrates that during the PHΦ of the MIO cycle, the data from the memory is accessed and place on the bus; during the PH1 of the MIO cycle, the data sits on the bus; and during the PH2 of the MIO cycle, the data on the bus is uploaded or read. Thus, the memory is only access once per MIO cycle and fails to anticipate accessing the unified memory, a second time, with a data access during execution of the last instruction of the loop, as set forth by independent claim 13.

With respect to dependent claims 2-5, 7, 8, 10-12, and 14, the Applicant, for the sake of brevity, will not address the reasons supporting patentability for these individual dependent claims, as these claims depend directly or indirectly from allowable independent claims 1, 8, 9, and 13. The Applicant reserves the right to address the patentability of these dependent claims at a later time, should it be necessary.

Accordingly, in view of all the reasons set forth above, the Examiner is respectfully requested to reconsider and withdraw this rejection.

CONCLUSION

Accordingly, in view of all the reasons set forth above, the Examiner is respectfully requested to reconsider and withdraw all the present rejections. Also, an early indication of allowability is earnestly solicited.

Respectfully submitted,

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